Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A method of decoding MPEG data comprising a plurality of macroblocks, each macroblock comprising a header and block layer data, said method comprising:

decoding the header of at least one macroblock using a first processing element; and

decoding the block layer data of said at least one macroblock using a second processing element.

2. (New) The method of claim 1, further comprising:

receiving a plurality of rows of the MPEG data, each row comprising the plurality of macroblocks,

wherein decoding the header comprises decoding the header of a first macroblock on a first one of the plurality of rows while concurrently decoding the block layer data of a second macroblock on a second one of the plurality of rows.

3. (New) The method of claim 2, further comprising providing the block layer data of the first macroblock to the second processing element after decoding the header of the first macroblock.

4. (New) The method of claim 1 wherein at least one of decoding the header and decoding the block layer data comprises variable length decoding.

5. (New) The method of claim 2, wherein receiving a plurality of rows of the MPEG data comprises receiving the plurality of rows of the MPEG data from memory.

6. (New) The method of claim 2, wherein receiving a plurality of rows of the MPEG data comprises receiving HDTV video data.

7. (New) The method of claim 1, further comprising:

decoding the header of at least one other macroblock using a third processing element concurrently with decoding of the header of said at least one macroblock using the first processing element; and

decoding the block layer data of said at least one other macroblock using a fourth processing element concurrently with decoding of the block layer data of said at least one macroblock using the second processing element.

8. (New) An MPEG decoding system for decoding MPEG data comprising a plurality of macroblocks, each macroblock comprising a header and block layer data, said system comprising:

a first processing element for decoding the header of at least one macroblock; and

a second processing element for decoding the block layer data of said at least one macroblock.

9. (New) The MPEG decoding system of claim 8, wherein the MPEG data is organized into a plurality of rows, each row comprising the plurality of macroblocks, and

wherein the first processing element decodes the header of a first macroblock on a first one of the plurality of rows, while the second processing element concurrently decodes the block layer data of a second macroblock on a second one of the plurality of rows.

10. (New) The MPEG decoding system of claim 8, wherein the system is implemented on an integrated circuit chip.

11. (New) The MPEG decoding system of claim 9, wherein the MPEG data comprises MPEG-2 video data and each row comprises at least one SLICE comprising the macroblocks.

12. (New) The MPEG decoding system of claim 8, further comprising a switch wherein the first processing element decodes the header of said at least one macroblock and the switch provides the block layer data of said at least one macroblock to the second processing element for decoding.

13. (New) The MPEG decoding system of claim 11 wherein the first macroblock is from a first SLICE and the second macroblock is from a second SLICE.

14. (New) A MPEG decoding system of claim 8, further comprising

a third processing element for decoding the header of at least one other macroblock concurrently with decoding the header of said at least one macroblock using the first processing element; and

a fourth processing element for decoding the block layer data of said at least one other macroblock concurrently with decoding the block layer data of said at least one macroblock using the second processing element.

15. (New) The MPEG decoding system of claim 8, wherein at least one of the first and second processing elements comprises a variable length decoder.

16. (New) The MPEG decoding system of claim 8, further comprising a video decoding engine for reading the MPEG data from memory and providing the MPEG data to the first processing element.

17. (New) The MPEG decoding system of claim 8 wherein the MPEG data comprises at least one HDTV video data.

18. (New) A video and graphics system comprising:

a transport processor for receiving one or more MEPG data streams and for extracting MPEG video data, the MPEG video data being organized into a plurality of rows, each row comprising a plurality of macroblocks, each macroblock having a header and block layer data;

a video decoder for decoding the MPEG video data to generate decoded video data, said video decoder comprising a first processing element for decoding the header and a second processing element for decoding the block layer data; and

a video compositor for blending the decoded video data with graphics,

wherein the first and second processing elements concurrently decode at least two rows of the MPEG video data.

19. (New) The video and graphics system of claim 18, wherein the transport processor, the video decoder, and the video compositor are integrated on an integrated circuit chip.

20. (New) The video and graphics system of claim 18, wherein the video decoder further comprises a third processing element for decoding the header and a fourth processing element for decoding the block layer data, wherein the third and fourth processing elements concurrently decode at least two other rows of the MPEG video data, concurrently with decoding the at least two rows using the first and second processing elements.